MEB90500 - E1

Customer Evaluation Kit

Advance Information

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Ordering Information

MEB90500 - E1

Features

- Allows Mitel customers to evaluate the MT90500AL device
- Demonstrates the advantages of Mitel AAL1 solution
- Eases bench-top prototyping to reduce development risk
- Provides a highly functional graphical user interface (GUI) in Windows NT
- Provides built-in logic for 155 Mbps, SONET STS-3C optical interface
- PLL connectivity for clock recovery
- Works with ISA-compatible cards for PC platforms
- Windows NT operating system
- Built-in connectors include: MT90500 UTOPIA L1 signals, MT90500 external SSRAM interface, PLL signals, MT90500 CPU bus header, MT90500 JTAG lines, 40-pin MVIP header for external TDM bus connection
- Wire-wrap area
- Includes Mitel MT90820 digital cross-point for TDM pattern generation
- Includes Mitel MT9160 codec to establish voice path
- This kit includes: handset connector for voice over ATM demo, 2 cards with 155 Mbps access rate and optical cable for interconnecting 2 cards
- Includes Mitel MT9041 PLL to implement clock recovery

Introduction

This document describes a kit containing printed circuit boards and sample software to be provided to Mitel MT90500 customers.

The package containing the card, example software, windows-based GUI and installation and description documentation is referred to as the MT90500 Customer Evaluation Kit (MCEK), from now on in this document.

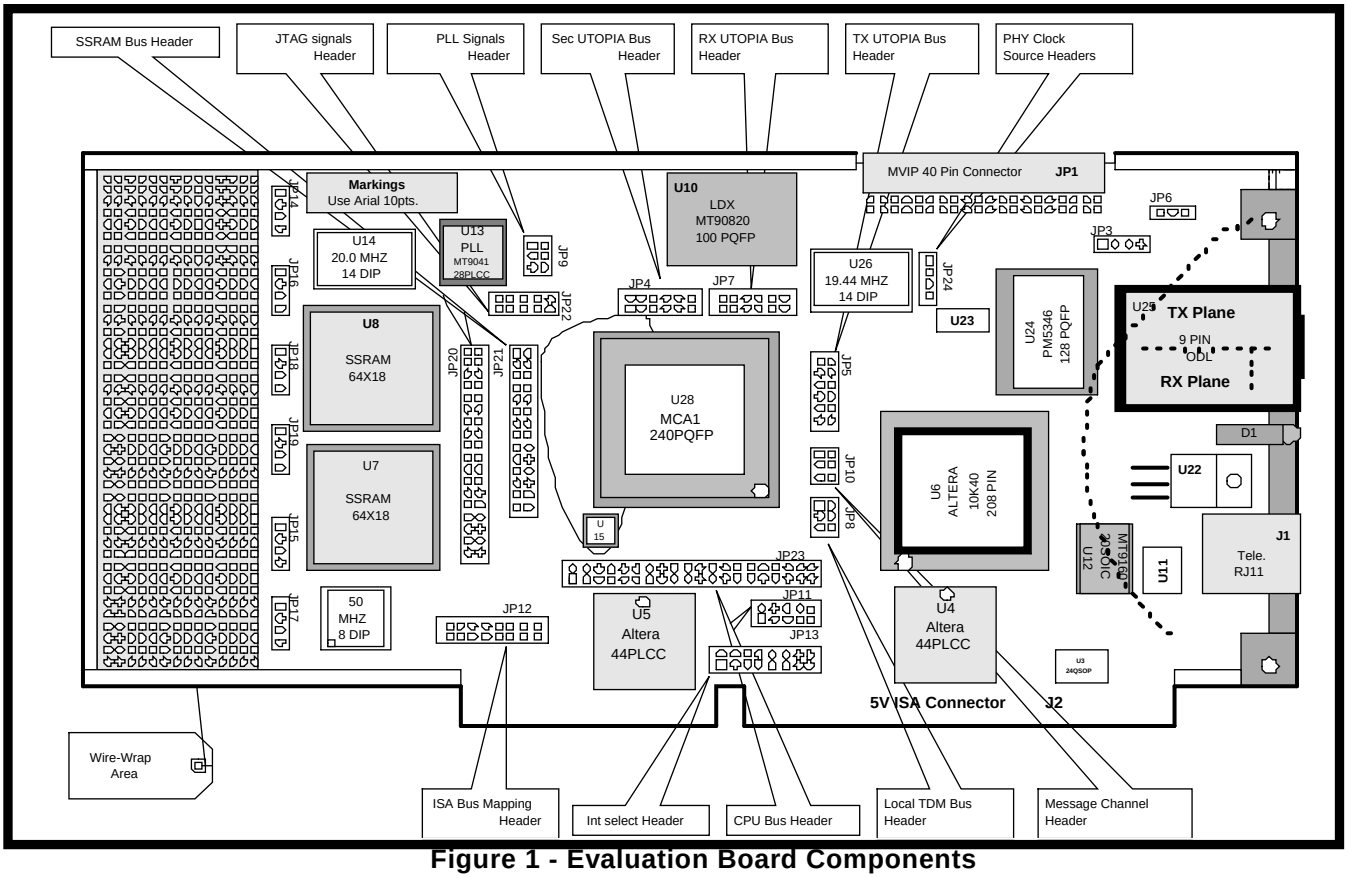

Figure 1 - Evaluation Board Components

Functional Requirements

Interface and Mechanical - this evaluation kit offers two PC-compatible boards with an ISA interface. The boards are fitted with an MVIP 40-pin connector, one RJ-11 jack for handset connection, and an optical module connector for the ATM 155 connection.

Hardware

Figure 1 outlines the physical characteristics of each MT90500 Evaluation card available in the kit.

The evaluation board is a PC-compatible 8/16-bit ISA board which provides the following interfaces:

- ATM155 MMF optical interface (ATM)
- MVIP compatibility (TDM)
- Handset Connector (Local TDM)

The specific components used are shown in Figure 1. The FPGA module emulates a Motorola/Intel processor via the ISA bus interface. This module emulates the functionality of a µprocessor and integrates all the other logic functions that are required to operate the board. It provides the necessary control for the operation of the Mitel codec (MT9160), LDX (MT90820) and external PLL (MT9041) as required.

The Mitel MT90820 LDX device allows the user to generate 64 kbps or nx64 kbps patterns to the MT90500 device, at 2.048, 4.096 and 8.192 Mbps.

The card contains an MT9160 codec interfacing with a telephone handset for demo purposes. A GUI interface is provided to operate the codec.

The MCEK is provided with two Synchronous SRAM (64K x 18) used by the MT90500 to externally store its control and data structures.

The MCEK is built with the tools necessary to exercise directly most of the MT90500 functionality:

- µprocessor interface (headers on control signals)
- external SSRAM interface
- TDM interface (external via the MVIP connector; local via headers)
- UTOPIA interface (primary and auxiliary interface headers)
- JTAG port (headers)
- TDM clock recovery and generation

The MCEK also provides the customer with the ability to use the following clock modes:

- Adaptive
- Freerun
- Synchronized to the 155Mbps PHY device (receive only)

Note: For SYNC to PHY modes, the MCEK allows the customer to access the 8kHz output from the PHY chip.

In addition, this kit contains a software algorithm for an adaptive clock recovery method.

In regards to clock generation and recovery, the cards can either generate clocks in master mode or receive input clocks in slave mode.

Software, Device Drivers

Three software modules are provided:

- A demonstration program which allows audio communications between two cards connected back to back via an ATM crossover cable or an ATM switch. The audio communication will be provided on each card via a telephone handset (codec on local bus). The software demonstrates how to set up one channel per VC in structured data transfer (SDT) mode. The clock mode (one of the 3 mentioned above) can be selected by the user. This demonstration program also allows the user to configure the MT90500 for multiple channels per VC in structured data transfer (SDT) mode or pointer-free mode, including the option for the clock mode selection. The pertinent documented C source code for this demo software is provided. This software runs under Windows NT.
- A demonstration program showing the power of the MT90500. To accomplish this objective, the application transmits 1024 channels simultaneously. The pertinent documented C source code for this demonstration is provided. The driver initializes the card, including the FPGA.
- A diagnostic module which provides access to registers within the Mitel MT90500 and its external memory. The diagnostic software is able to run while the other software is operating. This software runs under Windows NT.

Handset Connection

A simple handset connection using the Mitel MT9160 codec is used.

MCEK Contents

The MCEK consists of the following items:

- two (2) MT90500 Evaluation Boards
- one (1) ATM cross-over cable
- two (2) handsets
- 3.5" labeled diskettes containing the Windows NT binary software and the three documented demonstration programs in source code ('C')
- a documentation manual containing the kit installation and configuration instructions and board schematics

Warranty Terms

The following terms are applicable to this product:

Warranty: 30 days. Orders are Non Cancellable/Non Returnable. This engineering product is for technical evaluation only. Out of box failures will be replaced upon return of defective product, within 60 days from the day of return. Physical alterations or modifications will void this warranty.

Notes: